REPAIR OF THE HP 8640 SIGNAL GENERATOR HIGH-SPEED DIVIDER CIRCUITS

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The Hewlett-Packard type 8640 is a high-quality signal generator covering the range of 0.5 to 512 MHz. The HP8640 was designed circa 1970 as the state-of-the-art and marketed through the mid 1980s, to be replaced by synthesized signal generators. Official parts support was discontinued in 1991 and HP's stocks ran out several years later. The HP8640 was (and still is) exceptional for its spectral purity due to its cavity oscillator and divider design. Today there are many low-phase-noise applications for which a synthesizer is unsuitable and the HP8640 is still the generator of choice.

The 8640 is configured as a 256 to 512MHz cavity oscillator followed by a bank of successive divide-by-two circuits. Switch-selected banks of filters strip away the harmonics left by the divider chain, resulting in a very clean sine-wave output. Frequency readout and locking capability are provided by a digital counter operating directly off of the 256 to 512MHz oscillator output.

It is clear that the 8640 design relied heavily on the availability of high-speed dividers that could operate to at least 512 MHz. This capability was not available in commercial emitter-coupled logic families available at the time from Motorola and others, so HP fabricated their own in a process they dubbed "EECL". It is one of these dividers in the counter unit that failed in 8640 S/N 1734A07011. The HP part number is 1820-0736, a divide-by-two flip-flop with a two-input OR gate on the toggle input. When queried today, the 1820-0736 is not in HP's data base of available parts even though it was widely used in the HP8640 generator, HP5328 counter and probably other instruments in the RF arena.

HP's EECL logic family appears to have logic levels of zero and –0.8 volts and operates off a –5.2V power supply. The ECL logic families available today have logic levels of –1.0 and –1.6 V, so some interfacing must be done to incorporate a modern part. Luckily the power supply of the HP8640 is compatible with some modern ECL circuits.

After a brief search, I chose a Motorola MC100EL31D, a single D type flip-flop. Unfortunately, the 31D is available only in an eyesight-destroying surface-mount 8 pin SOIC package. Since the 31D is rated to 2.8GHz, careful layout and construction are needed to ensure proper operation. The OR-gate input configuration of the original IC could be deleted with minimal impact on the functionality of the counter unit in this case.

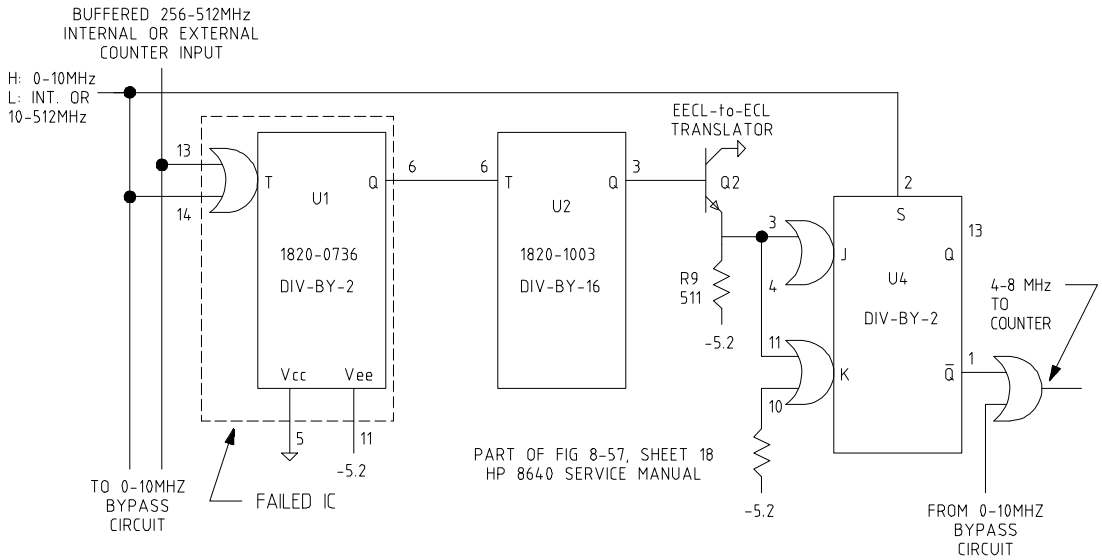

Figure 1: Existing HP 8640 counter input circuit with failed IC

Figure 1 shows the existing circuit of the counter input section. A buffer stage and input-selection relay precedes the “Buffered 256-512MHz….” input and the “4-8MHz to Counter” output feeds a low-frequency counter, display and frequency-locking system implemented in TTL.

Figure 2 shows the replacement circuit. The original circuit has two frequency ranges, 0-10MHz and 10-512 MHz. The high-speed circuits operate only in the 10-512MHz or internal modes. The high-speed circuit is disabled in the 0-10MHz mode by two methods; one by gating OFF the first divider with its OR-toggle input, the second by disabling the last divide-by-2 with its SET input. The OR-gate of the first method appears redundant with the second and was not implemented in the repair.

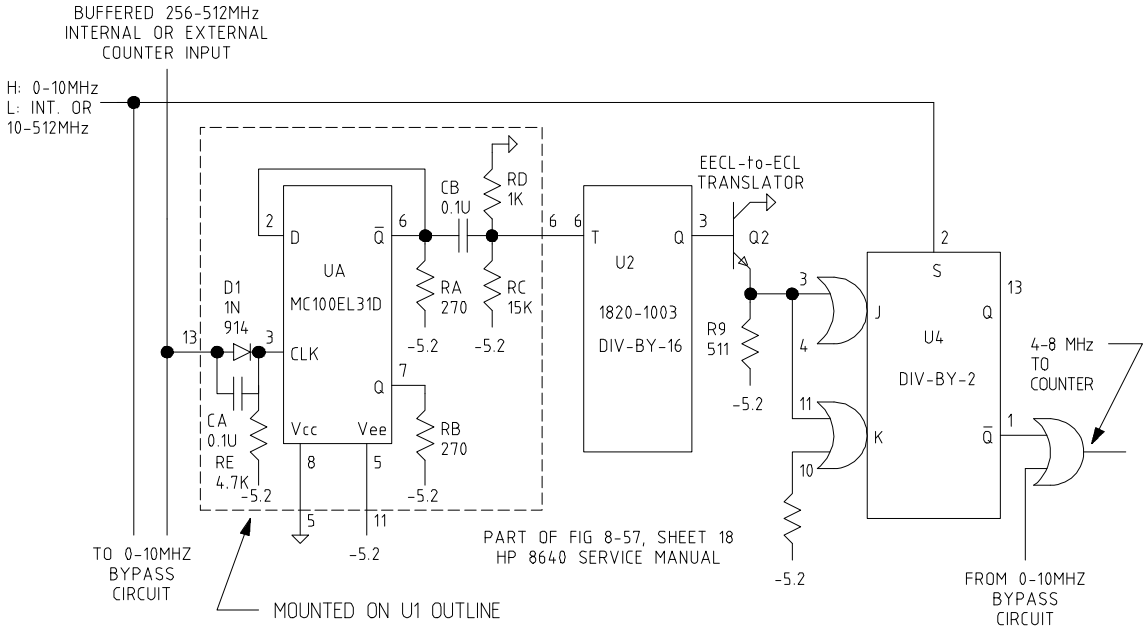

Figure 2: Replacement U1 and logic level interface circuit

Diode D1 and bypass capacitor CA couple the input RF signal to the CLK input of the MC100EL31D while translating EECL logic levels to ECL. RE biases diode D1 ON to about 0.6V. RA and RB load the outputs to about 20mA. This is required for proper toggling operation. RC and RD bias U2’s EECL input to about -0.37V (including about 60uA input current), roughly the mid-point of its logic levels. CB couples in the AC component of the switching waveform.

I was unable to investigate the quality of the switching waveforms due to the lack of a suitable high-frequency oscilloscope. However, the circuit works correctly from band-edge to band-edge with no holes. Lead length, layout and grounding are critical to any fast circuit, this is no exception. Implementation was relatively straight forward despite the small size of the SOIC-8 package of the new IC.

The original U1 IC was removed. The circuit was built in layers, with the IC mounted over a small copper tape ground-plane insulated with Mylar tape. A dot of cyanoacrylate glue held UA in position over the ground plane. Soldering heat did not appear to damage the tape if done quickly enough. The entire circuit fit within the outline of the original DIP-16 package including a pair of –5.2V tab connections for the 1820-0736’s substrate. Short lengths of 30-ga wire-wrap wire were used for interconnection. The pin 2 to pin 6 jumper may be installed on UA before it is mounted, if desired. The construction is described in Figure 3A through 3E.

It may be possible to use a variant of the technique described here in the frequency divider circuits of the 8640, and in other instruments such as Option C of the HP5328 counter to effect a repair.

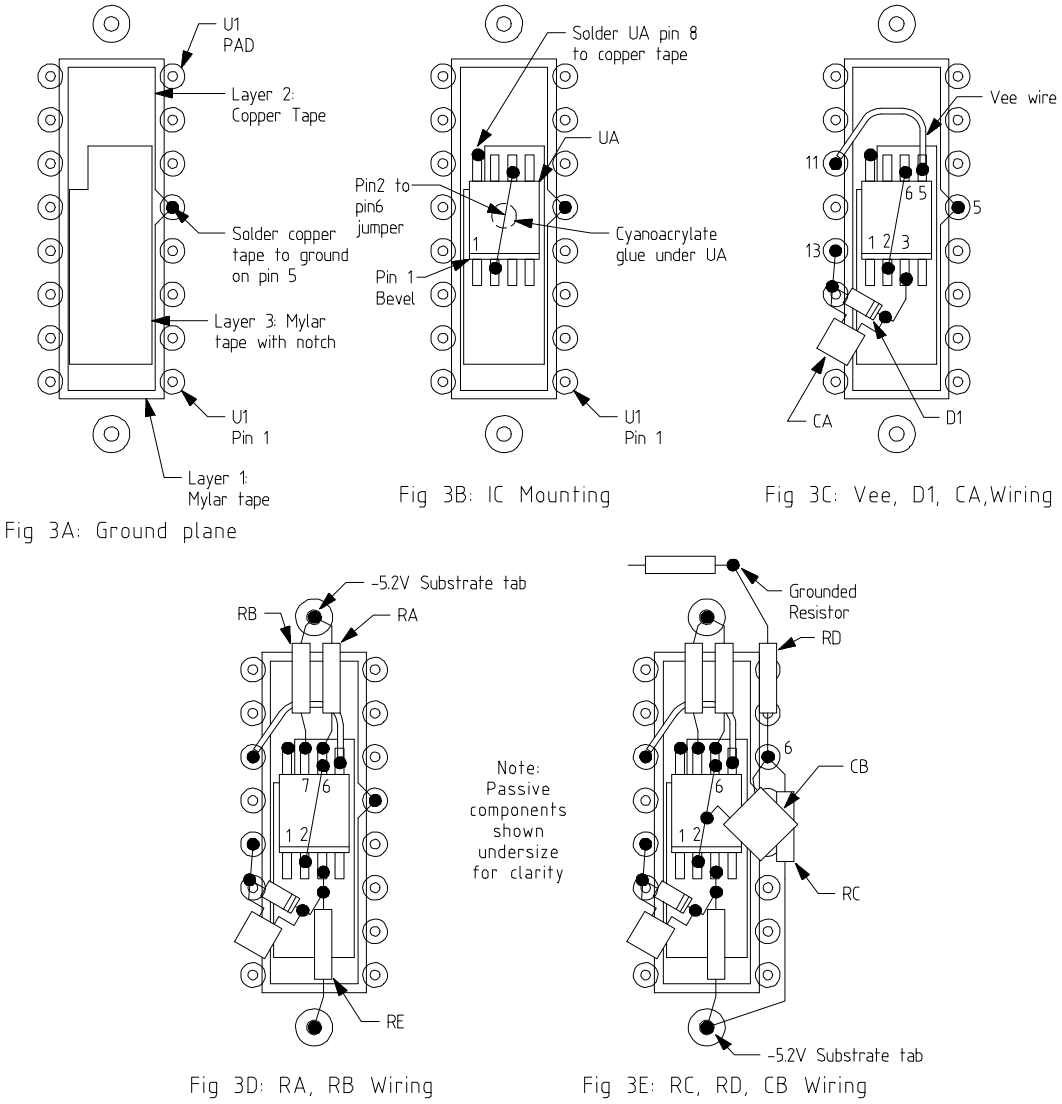

Figure 3: Component Layout

Thanks are due to Elmer Fredd for encouragement and allowing me the time to develop and implement the repair, John Gennuso for trying his best to locate the original part, and Marilyn Hondorp for obtaining the substitute parts faster than I could imagine.